

动态特性Dynamic Characteristics (note4)						
输入电容Input Capacitance	C _{iss}	V _{DS} = 10V, V _{GS} =0V, f=1MHz	--	700	--	pF
输出电容Output Capacitance	C _{oss}		--	92	--	pF
反向传输电容 Reverse Transfer Capacitance	C _{rss}		--	80	--	pF
开关特性Switching Characteristics (note 4)						
开启延迟时间Turn-on delay time	t _{d(on)}	V _{DD} = 10V, I _D = 1A, R _G = 3.3Ω, V _{GS} = 4.5V	--	5	--	ns
开启上升沿时间Turn-on rise time	t _r		--	14.4	--	ns
关断延迟时间Turn-off delay time	t _{d(off)}		--	30	--	ns
关断下降沿时间Turn-off fall time	t _f		--	9.2	--	ns
总栅极电荷Total Gate Charge	Q _g	V _{DS} = 10V, I _D =5A, V _{GS} =4.5V	--	9.4	--	nC
栅源电荷Gate-Source Charge	Q _{gs}		--	0.6	--	nC
栅漏电荷Gate-Drain Charge	Q _{gd}		--	2	--	nC

***Notes :**

1. Repetitive rating: Pulse width limited by maximum junction temperature
2. Surface Mounted on FR4 board, t≤10 sec.
3. Pulse test : Pulse width≤300μs, duty cycle≤2%.
4. Guaranteed by design, not subject to production.

典型特性曲线 Typical characteristics

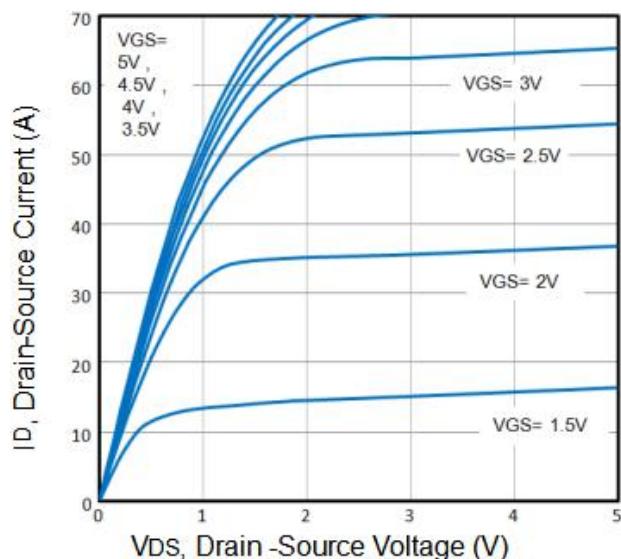


Fig1. Typical Output Characteristics

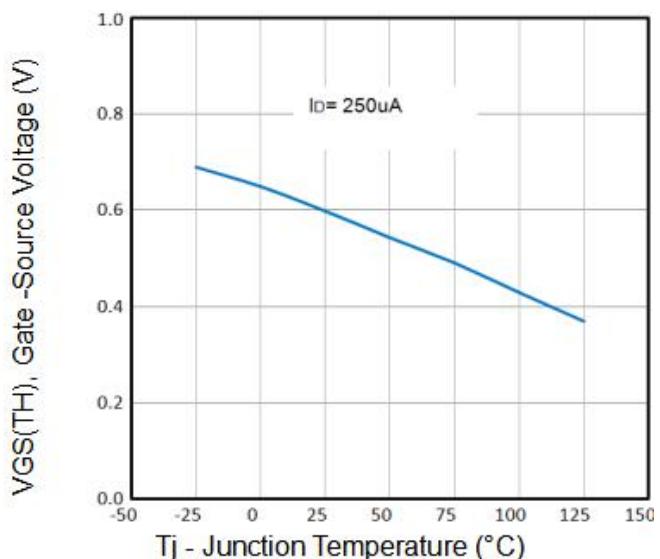


Fig2. $V_{GS(TH)}$ Voltage Vs. Temperature

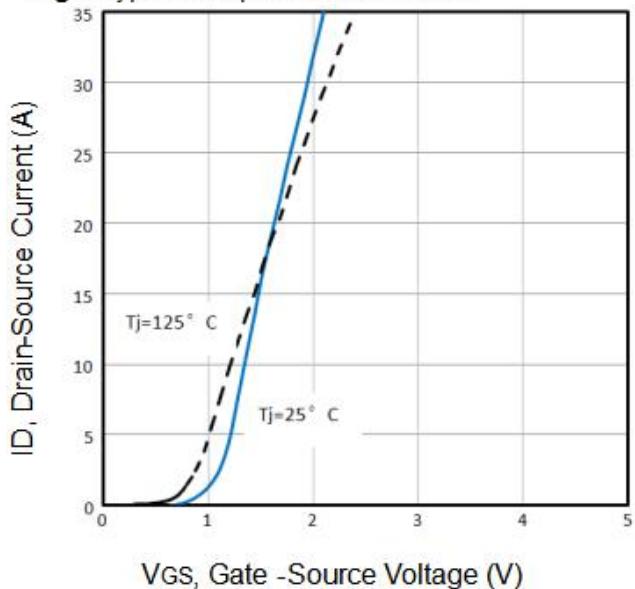


Fig3. Typical Transfer Characteristics

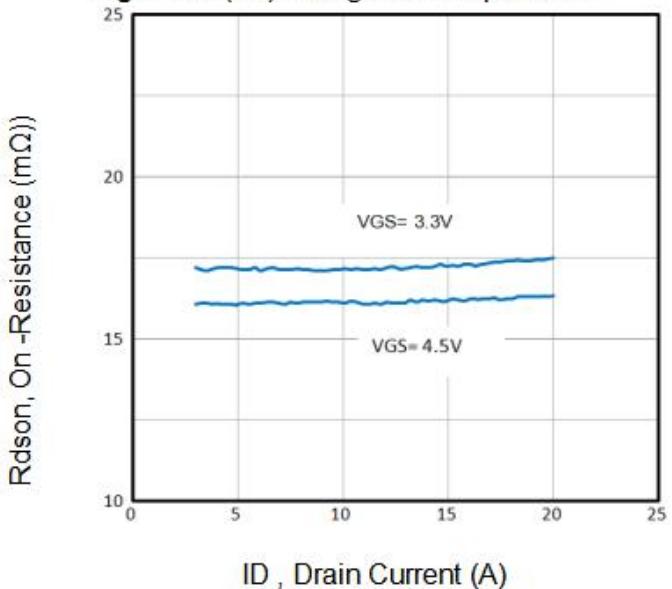


Fig4. On-Resistance vs. Drain Current and Gate

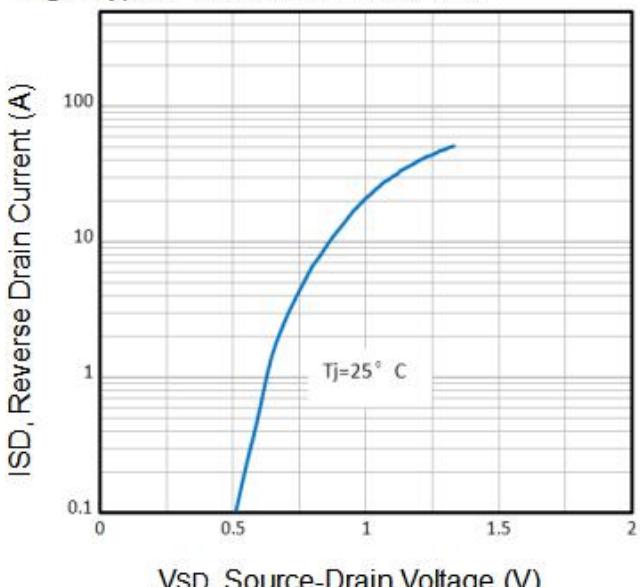


Fig5. Typical Source-Drain Diode Forward Voltage

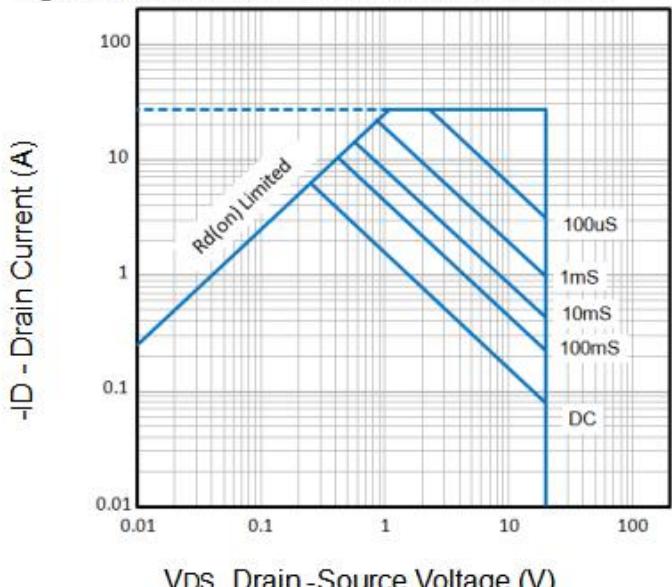
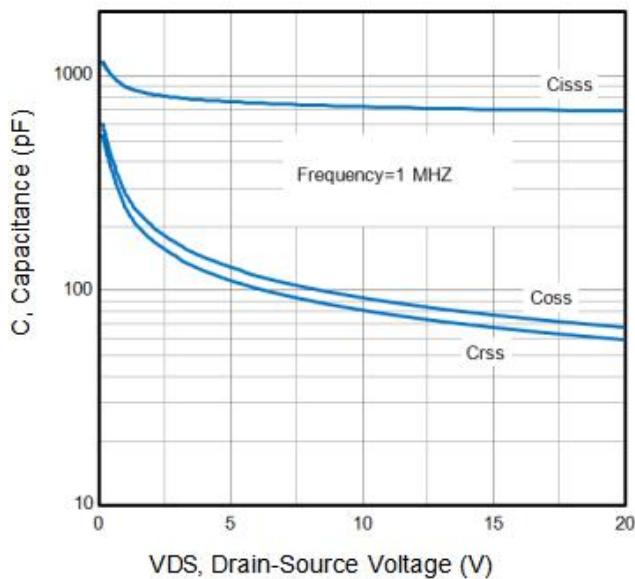
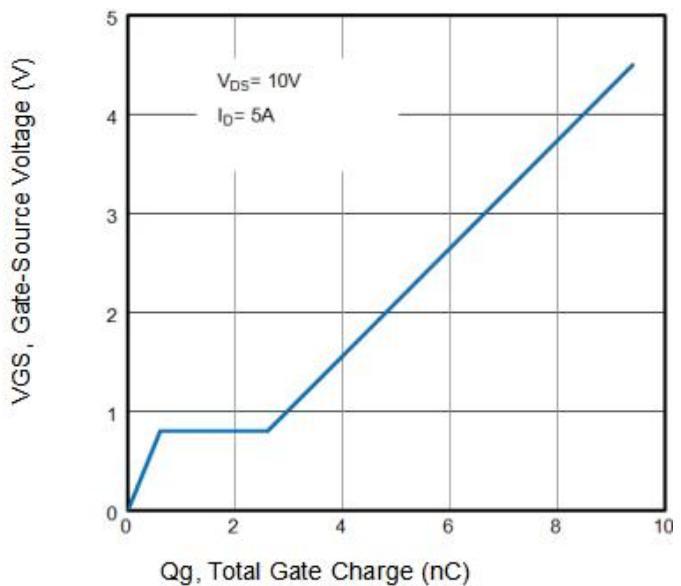
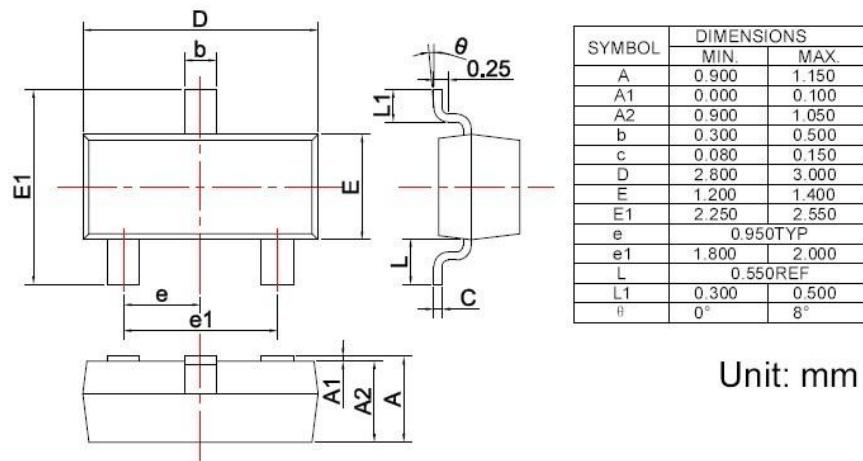


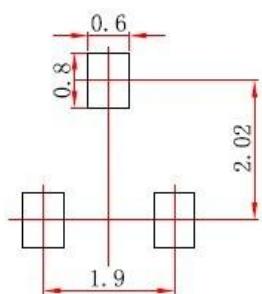
Fig6. Maximum Safe Operating Area

**Fig7.** Typical Capacitance Vs. Drain-Source Voltage**Fig8.** Typical Gate Charge Vs. Gate-Source Voltage

封装外形图 SOT-23 Package Outline Dimensions



焊盘设计参考 Precautions: PCB Design



Note:
 1. Controlling dimension: in millimeters.
 2. General tolerance: ± 0.05 mm.
 3. The pad layout is for reference purposes only.